ASSIGNMENT # 4 (15 POINTS)

1. A) Describe in your own words, why would we need to maintain the PDN impedance below the target impedance.

B) If the voltage rail (Vdd) runs on 3.3V and the maximum allowed ripple is 5% and maximum power the chip draws is 5W, calculate the target impedance.

1. A) Explain why the board level target impedance can be limited only up to 100MHz.

B) Explain the role of decoupling capacitors in PDN

1. A) Calculate loop inductance of a 50-ohm, 0.2-inch long microstrip trace.

B) Calculate loop inductance between two 50mil long vias of 5mils in diameter separated by 50mils.

C) Calculate loop inductance between two planes of 5-inch length and 2mils of spacing between them.

1. Calculate spreading loop inductance between two via contacts in a pair of planes with dielectric thickness of 4 mils, the distance between the via centers is 10 mils and the diameter of the vias is 5mil.
2. How many capacitors are needed in parallel to meet the target impedance of 0.01Ohm at Fmax: 100MHz with each capacitor having ESL of 1nH.